Listing of Claims

1. (Previously Presented) A noise suppression method, comprising:

generating a frequency signal from a PLL based on a reference signal; and

removing noise from the frequency signal by setting a frequency divider in a feedback loop of the PLL to a value which shifts a spurious signal of a predetermined order outside a loop bandwidth of the PLL, wherein setting the frequency divider includes:

adjusting at least one of a swallow counter and a program counter in the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL.

2. (Original) The method of claim 1, wherein the loop bandwidth is defined by a cutoff frequency of a loop filter in the PLL.

3. (Original) The method of claim 1, wherein the loop bandwidth corresponds to a frequency range that lies between the frequency signal generated from the PLL and a cutoff frequency of a loop filter in the PLL.

4. (Previously Presented) The method of claim 1, wherein said noise is removed by:

adjusting at least one of the swallow counter and program counter to a value which shifts a first-order spurious signal outside the loop bandwidth of the PLL.

5. (Canceled)

6. (Previously Presented) The method of claim 1, wherein at least one of the swallow counter and program counter is set by a Sigma-Delta modulator.

7. (Canceled)

8. (Previously Presented) The method of claim6, further comprising:

computing a modulation ratio of the Sigma-Delta modulator based on the loop bandwidth of the PLL; and

setting the value of at least one of the swallow counter and program counter based on the modulation ratio computed for the Sigma-Delta modulator.

9. (Previously Presented) The method of claim 56, wherein values for the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL.

10. (Previously Presented) The method of claim 9, wherein the frequency signal of the PLL (f_{VCO}) is generated in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$$

, where f_{ref} is the reference signal, R is a value of a reference signal divider, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ration of the Sigma-Delta modulator, and K is a value of the prescaler in the pulse swallow frequency divider.

11. (Original) The method of claim 9, further comprising:

modulating the reference signal input into the PLL.

12. (Previously Presented) The method of claim 11, wherein the frequency signal of the PLL (f_{VCO}) is generated in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{mod}}{D_{mod}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$$

where f_{ref} is the reference signal, R is a value of a reference signal divider N_{mod} and D_{mod} define a modulation ratio for the reference signal, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is the value of a prescaler in the pulse swallow frequency divider.

13. (Original) The method of claim 11, further comprising:

using the modulated reference signal as a comparison signal for the PLL as long as harmonics of the modulated reference signal and the unmodulated reference signal are not coincident.

14. (Original) The method of claim 1, wherein the spurious signal is generated by a mismatch relating to at least one of a phase and frequency detected and a charge pump of the PLL.

15. (Canceled)

16. (Canceled)

17. (Previously Presented) A frequency generator, comprising:

a phase-locked loop which generates a frequency signal based on a reference signal; and

a noise suppressor which shifts a spurious signal of a predetermined order outside a loop bandwidth of the PLL, wherein the noise suppressor includes a frequency divider in a feedback loop of the phase-locked loop, and a controller which sets the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop, and

wherein the frequency divider includes a swallow counter and a program counter and wherein values for the swallow and program counters are controlled based on a modulation ration of a Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

18 (Original) The frequency generator of claim 17, wherein the phase-locked loop includes a loop filter, and the loop bandwidth is defined by a cutoff frequency of the loop filter.

19. (Original) The frequency generator of claim 17, wherein the phase-locked loop includes a loop filter, and the loop bandwidth corresponds to a frequency range that lies between the frequency signal generated from the PLL and a cutoff frequency of the loop filter.

20. (Previously Presented) The frequency generator of claim 17, wherein said values of the swallow and program counters are controlled to shift a first-order spurious signal outside the loop bandwidth of the phase-locked loop.

21-25. (Cancelled)

26. (Previously Presented) The method of claim 25, wherein the PLL generates the frequency signal (f_{vco}) in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

27. (Previously Presented) The method of claim 25, further comprising:

a modulator which modulates the reference signal input into the phase-locked loop.

28. (Previously Presented) The frequency generator of claim 27, wherein the PLL generates the frequency signal in accordance with the following equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{mod}}{D_{mod}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$$

where f_{ref} is the reference signal, R is a value of a reference signal divider N_{mod} and D_{mod} define a modulation ratio for the reference signal, P is the value of the program counter, S is the value of the

swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is the value of a prescaler in the pulse swallow frequency divider.

29. (Original) The frequency generator of claim 27, wherein the modulated reference signal is used as a comparison signal for the PLL as long as harmonics of the modulated reference signal are not coincident with harmonics of the unmodulated reference signal.

30. (Original) The frequency generator of claim 27, wherein the spurious signal is generated from a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

31. (Canceled)

32. (Canceled)

33. (Previously Presented) A system for controlling a PLL, comprising:

a divider which divides a frequency signal output from the PLL; and

a controller which sets the divider to a value which shifts a spurious noise signal of a predetermined order outside the loop bandwidth of the PLL, wherein the divider includes a swallow counter and a program counter, and

wherein values for the swallow and program counters are controlled based on a modulation ration of a Sigma-Delta modulator, said values for the swallow and program counters being controlled to generate said value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop.

34. (Original) The system of claim 33, wherein the loop bandwidth is defined by a cutoff frequency of a loop filter of the PLL.

35. (Original) The system of claim 33, wherein the loop bandwidth corresponds to a frequency range that lies between the frequency signal and a cutoff frequency of a loop filter in the PLL.

36. (Previously Presented) The system of claim 33, wherein said values of the swallow and program counters shift a first-order spurious signal outside the loop bandwidth of the phase-locked loop.

37-39. (Cancelled)

40. (Previously Presented) The system of claim 33, wherein the controller controls the PLL to generate the output frequency signal in accordance with the equation:

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{mod}}{D_{mod}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$$

where f_{ref} is the reference signal, R is a value of a reference signal divider, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is a value of a prescaler in the pulse swallow frequency divider.

41. (Previously Presented) The system of claim 33, wherein the controller includes:

a modulator which modulates a reference signal of the PLL.

42. (Previously Presented) The system of claim 41, wherein the controller controls the PLL to generate the output frequency signal based on the equation

$$f_{vco} = \left(\frac{f_{ref}}{R}\right)\left(\frac{N_{mod}}{D_{mod}}\right)\left((K \cdot P + S) + \left(\frac{N_{\Sigma\Delta}}{D_{\Sigma\Delta}}\right)\right)$$

where f_{ref} is the reference signal, R is a value of a reference signal divider N_{mod} and D_{mod} define a modulation ratio for the reference signal, P is the value of the program counter, S is the value of the swallow counter, $N_{\Sigma\Delta}$ and $D_{\Sigma\Delta}$ is the modulation ratio of the Sigma-Delta modulator, and K is the value of a prescaler in the pulse swallow frequency divider.

43. (Original) The system of claim 41, wherein the modulated reference signal is used as a comparison signal of the PLL as long as the harmonic of the modulated reference signal is not coincident with a harmonic of unmodulated reference signal.

44. (Original) The system of claim 33, wherein the spurious noise signal is generated from a mismatch relating to at least one of a phase and frequency detector and a charge pump of the PLL.

45. (Previously Presented) The method of claim 1, wherein the spurious signal is generated from a mismatch in at least one of a charge pump and phase/frequency detector in the PLL.

46. (Previously Presented) The method of claim 45, wherein the mismatch in the charge pump includes a mismatch between UP and DOWN current sources.

47. (Previously Presented) The method of claim 45, wherein the spurious signal is generated from a mismatch between UP and DOWN signal paths in the phase/frequency detector.

48. (Previously Presented) The method of claim 1, wherein the value of the frequency divider is set based on a modulation ratio of a Sigma-Delta modulator for removing the spurious signal.

49. (Previously Presented) A noise suppression method, comprising:

generating a frequency signal from a PLL based on a reference signal; and

removing noise from the frequency signal by setting a frequency divider in a feedback loop of the PLL to a value which shifts a spurious signal of a predetermined order outside a loop bandwidth of the PLL, wherein the frequency divider is a pulse swallow frequency divider which includes a swallow counter and a program counter, and wherein values for at least one of the swallow and program counters are controlled based on the modulation ratio of the Sigma-Delta modulator.

50. (Previously Presented) The method of claim 49, wherein a numerator of the modulation ratio ($N_{\Sigma\Delta}$) is at least 50% of a denominator of the modulation ratio ($D_{\Sigma\Delta}$).

51. (Previously Presented) The method of claim 50, further comprising:

modulating the reference signal into the PLL with a reference modulator, wherein the reference modulator has a modulation ratio (N_{mod}/D_{mod}) such that N_{mod} is at least 50% of D_{mod}.

52. (Canceled)

53. (Previously Presented) The method of claim 1, further comprising:

shifting the reference signal to a fractional fixed value for input into a phase/frequency detector of the PLL, said fractional fixed value further shifting the spurious signal

of said predetermined order.

54. (Previously Presented) The frequency generator of claim 17, further comprising:

a frequency shifter which shifts the reference signal to a fractional fixed value for input into a phase/frequency detector of the PLL, said fractional fixed value further shifting the spurious signal of said predetermined order.

55. (Canceled)

56. (Previously Presented) The method of claim 1, wherein the swallow counter and program counter are both adjusted to shift the spurious signal of said predetermined order outside the loop bandwidth of the PLL.